Negative Capacitance Carbon Nanotube FETs

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Abstract—As continued scaling of silicon FETs grows increasingly challenging, alternative paths for improving digital system energy efficiency are being pursued. These paths include replacing the transistor channel with emerging nanomaterials (such as carbon nanotubes), as well as utilizing negative capacitance effects in ferroelectric materials in the FET gate stack, e.g., to improve sub-threshold slope beyond the 60 mV/decade limit. However, which path provides the largest energy efficiency benefits—and whether these multiple paths can be combined to achieve additional energy efficiency benefits—is still unclear. Here, we experimentally demonstrate the first negative capacitance carbon nanotube FETs (CNFETs), combining the benefits of both carbon nanotube channels and negative capacitance effects. We demonstrate negative capacitance CNFETs, achieving sub-60 mV/decade sub-threshold slope with an average sub-threshold slope of 55 mV/decade at room temperature. The average on-current ($I_{ON}$) of these negative capacitance CNFETs improves by 2.1x versus baseline CNFETs, (i.e., without negative capacitance) for the same off-current ($I_{OFF}$). This work demonstrates a promising path forward for future generations of energy-efficient electronic systems.

Index Terms—Negative capacitance, carbon nanotube, field-effect transistors, very-large-scale integration.

I. INTRODUCTION

While scaling FETs has improved energy efficiency of digital very-large-scale integrated (VLSI) circuits for decades (e.g., Dennard Scaling [1]), continued scaling is resulting in diminishing returns [2]. For instance, circuit supply voltage ($V_{DD}$) no longer scales according to Dennard Scaling, in part due to the sub-threshold slope (SS) limit of 60 mV/decade (at temperature $= 300$°K) for conventional FETs (which in itself is difficult to achieve due to short-channel effects) [3], [4].

To overcome these challenges, multiple orthogonal paths are being pursued. One promising option is to replace today’s silicon-based FET channels with ultra-thin body nanomaterials; for instance, carbon nanotubes (CNTs, Fig. 1b) can be used to realize carbon nanotube FETs (CNFETs, Fig. 1a), which offer superior electrostatic control vs. silicon-based FETs, simultaneously with superior carrier transport [5]. Another promising option is to introduce new materials into the FET gate stack; e.g., ferroelectric (FE) materials that exhibit negative capacitance (NC) can result in amplification of the electric field at the interface between the semiconductor channel and the gate oxide [6]. This allows the circuit supply voltage ($V_{DD}$) to decrease, thus lowering energy consumption while maintaining high effective gate-to-source voltage ($V_{GS,eff}$) for high drive current and high $I_{ON}/I_{OFF}$ ratio (e.g., to improve energy efficiency) [7]. Importantly, NC can be combined with CNTs to realize NC-CNFEFTs, the focus of this manuscript.

The schematic of an example NC-CNFEFT is shown in Fig. 1d (Fig. 1a: baseline CNFET: without negative capacitance). The gate stack (from bottom to top) consists of an external metal gate, a ferroelectric oxide, an internal metal layer, and a high-k gate oxide. Multiple parallel CNTs comprise the FET channel, whose conductance is modulated by the voltage of the internal metal layer; this layer serves to average the non-uniform charge in the NC-CNFEFT channel from source-to-drain under non-zero bias conditions, and presents an average charge to stabilize the ferroelectric capacitance in the negative capacitance state [8], [9]. The source, drain, and gate regions are defined using traditional photolithography.

Here, we experimentally demonstrate the first NC-CNFEFTs. For 100 single-CNT CNFETs (i.e., CNFETs with a single CNT in the channel region), we show that our NC-CNFEFTs improve SS from an average of 70 mV/decade (for the baseline CNFETs) to an average of 55 mV/decade (for the NC-CNFEFTs), contributing to an average $I_{ON}$ per CNT...
increase of $2.1 \times$ versus baseline CNFETs for the same average $I_{OFF}$.

II. FABRICATION PROCESS

Fig. 2 illustrates the fabrication flow for baseline CNFETs (Fig. 2a) and NC-CNFETs (Fig. 2b). We use a back-gate FET geometry (i.e., where the semiconducting channel of the FET is deposited over a pre-fabricated gate-stack), as it decouples the high temperature processing (>700 °C anneal) required for the ferroelectric material within the gate stack from the CNTs used as the channel [8]. The starting substrates for both baseline CNFETs and NC-CNFETs are silicon wafers with 800 nm of thermal SiO$_2$. For the back-gate, 40 nm of tungsten is defined through a lift-off process. For the NC-CNFET, a 10 nm ferroelectric dielectric is deposited, followed by a 8 nm tungsten metal layer. The ferroelectric dielectric is ~7% aluminum-doped hafnium oxide (7% Al:HfO$_x$), deposited through atomic layer deposition (ALD) over the bare tungsten metal gate for the baseline CNFET). The HfO$_x$ deposited over the ferroelectric oxide ensures stable operation (e.g., positive gate capacitance), by introducing a positive capacitance dielectric oxide in series with the ferroelectric dielectric layer and the semiconductor [9], [10]. The 1 nm Al$_2$O$_x$ provides an ideal surface for the subsequent transfer of CNTs over the channel region (after fabrication of the gate stack) [11]–[13]. Finally, platinum electrodes are deposited for source/drain.

III. NC-CNFET EXPERIMENTAL DEMONSTRATION

We provide results from 100 CNFETs: 50 baseline CNFETs and 50 NC-CNFETs. The channel length of the CNFETs is 1 µm, and the width is chosen to achieve ~1 CNT per CNFET (to compare the performance of each single CNT channel). Each CNFET is first measured to determine if it has a semiconducting or a metallic CNT in the channel bridging the source and drain metal contacts (we define metallic CNTs as CNT that result in CNFETs with $I_{ON}/I_{OFF} > 100$; for energy-efficient circuits, metallic CNTs would be removed using techniques described in ref. 16). After measuring all of the CNFETs, we image each CNFET using scanning electron microscopy (SEM) to confirm that only a single semiconducting CNT is within the channel of the CNFET. SEM and cross-section transmission electron microscopy (TEM) images of a typical fabricated NC-CNFET are shown in Fig. 4 (in the TEM, individual CNTs are not visible due to the CNTs being perpendicular to the cross-section).
of SS and $I_{ON}/I_{OFF}$ are shown in Fig. 6a and Fig. 6b respectively. The average SS improves from 70 mV/decade for baseline CNFET to 55 mV/decade for NC-CNFET. Due in part to the improved SS, the average $I_{ON}/I_{OFF}$ improves by 2.1× for the same $I_{OFF}$. These results experimentally verify the effectiveness of the ferroelectric oxide to amplify the voltage of the external metal gate onto the internal metal layer and achieve sub-60 mV/decade SS operation. Importantly, gate leakage ($I_{G}$, which must be limited for stable negative

capacitance operation [9]) is negligible ($|I_{G}| < 30$ pA) for both the baseline CNFETs and NC-CNFETs, as shown in Fig. 5b.

Fig. 7 shows a typical $I_{D} - V_{DS}$ characteristic for a NC-CNFET. Importantly, while the NC-CNFET exhibits the expected saturation current as the magnitude of $V_{DS}$ increases, it also exhibits negative output conductance (as shown in Fig. 7). This negative output conductance at high $V_{DS}$ magnitude (which has been observed in NC-FET experimental demonstrations and is consistent with the expected behavior in the compact model as shown in Fig. 8c [15]) introduces a fundamental trade-off for NC-FETs: due to the non-monotonic relationship between $I_{D}$ and $V_{DS}$ in NC-FETs [15], there can be hysteresis in logic gates made from NC-FETs (illustrated in Fig. 8) [22], [23]. This is typically undesirable for digital logic circuits as it can lead to various circuit problems (e.g., incorrect logic functionality). Thus, the positive and negative capacitance portions of the gate stack must be carefully co-optimized to maximize energy efficiency benefits while minimizing the hysteresis effect on logic gates.

IV. CONCLUSION

We have experimentally demonstrated the first NC-CNFETs, which achieve an average SS of 55 mV/decade (compared to 70 mV/decade for baseline CNFETs), and improve average $I_{ON}$ by 2.1× versus baseline CNFETs (for the same $I_{OFF}$). This work experimentally demonstrates a path for combining the benefits of both CNT channels with negative capacitance effects, for future generations of energy-efficient electronic systems.

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REFERENCES


